OMR Answer Sheet No.	Question Booklet Number
	3039

BCA (III Sem.) Examination, 2024-25

Booklet Series
B

Bachelor of Computer Application

Computer Organization and architecture

(To be filled by the Candidate / निम्न पूर्तियाँ परीक्षार्थी स्वयं भरें)

Roll No. (in figures)
अनुक्रमांक (अंकों में) _____

Roll No. (in words)
अनुक्रमांक (शब्दों में) _____

[Time : 2 : 00 Hours
[समय : 2 : 00 घण्टे

[Maximum Marks : 70
[अधिकतम अंक : 70

Name of Examination Centre
परीक्षा केन्द्र का नाम _____

_____
Signature of Invigilator
कक्ष निरीक्षक के हस्ताक्षर

Instructions to the Examinee :

1. Do not open the booklet unless you are asked to do so.
2. **The booklet contains 75 questions. Examinee is required to answer any 65 questions in the OMR Answer-Sheet provided and not in the question booklet. In case Examinee attempts more than 65 Questions, first 65 attempted questions will be evaluated. All questions carry equal marks.**
3. Examine the Booklet and the OMR Answer-Sheet very carefully before you proceed. Faulty question booklet due to missing or duplicate pages/questions or having any other discrepancy should be immediately replaced.

(Remaining Instructions on last page)

परीक्षार्थियों के लिए निर्देश :

1. प्रश्न-पुस्तिका को तब तक न खोलें जब तक आपसे कहा न जाए।
2. **प्रश्न-पुस्तिका में 75 प्रश्न हैं। परीक्षार्थी को किन्हीं 65 प्रश्नों को दी गई ओ०एम०आर० आन्सर-शीट पर ही हल करना है। परीक्षार्थी द्वारा 65 से अधिक प्रश्नों को हल करने की स्थिति में, प्रथम 65 उत्तरों को ही मूल्यांकित किया जायेगा। सभी प्रश्नों के अंक समान हैं।**
3. प्रश्नों के उत्तर अंकित करने से पूर्व प्रश्न-पुस्तिका तथा OMR उत्तर-पत्रक को सावधानीपूर्वक देख लें। दोषपूर्ण प्रश्न-पुस्तिका, जिसमें कुछ भाग छपने से छूट गये हों या प्रश्न एक से अधिक बार छप गये हों या किसी भी प्रकार की कमी हो, उसे तुरन्त बदल लें।

(शेष निर्देश अन्तिम पृष्ठ पर)

1. What is the purpose of device drivers in I/O organization?
   (A) Control the flow of data within the CPU
   (B) Translate high-level language code into machine language
   (C) Provide an interface between the operating system and hardware devices
   (D) Store frequently accessed data and instructions

2. What is parallel processing?
   (A) Processing data one after the other
   (B) Processing data simultaneously using multiple processors
   (C) Processing data using a single processor
   (D) Processing data using specialized hardware accelerators

3. Which of the following is a benefit of parallel processing?
   (A) Increased complexity of programming
   (B) Decreased computational speed
   (C) Increased throughput and performance
   (D) Reduced power consumption

4. What is meant by "task parallelism" in parallel processing?
   (A) Dividing a task into subtasks that can be executed concurrently
   (B) Running multiple tasks simultaneously on different processors
   (C) Running a single task across multiple processors
   (D) Synchronizing tasks to ensure correct execution order

5. What is "thread-level parallelism" in parallel processing?
   (A) Running multiple tasks simultaneously on different processors
   (B) Dividing a task into multiple threads that can be executed concurrently
   (C) Running a single task across multiple processors
   (D) Synchronizing tasks to ensure correct execution order

6. Which of the following is a type of architecture used in the computers now-a-days?
   (A) Microarchitecture
   (B) Harvard architecture
   (C) Von-Neumann architecture
   (D) System Design

7. Which of the following is used for binary multiplication?

(A) Restoring multiplication

(B) Booth's Algorithm

(C) Pascal's Rule

(D) Digit-by-digit multiplication

8. The operation that can be performed on the status register is

(A) Write operation

(B) Read operation

(C) Read and Write operation

(D) None of the mentioned

9. In tightly coupled system the microprocessor share--------

(A) Common clock

(B) Bus Control logic

(C) Common clock and bus control logic

(D) None of these

10. What is the hexadecimal representation of the binary number 101011?

(A) A3

(B) B5

(C) 2B

(D) 5A

11. Who is the father of computer?

(A) Charles Newman

(B) Charles Babbage

(C) Henry Babbage

(D) Henry luce

12. The data can be accessed from the disk using ----------

(A) Surface number

(B) Sector number

(C) Track number

(D) All of these

13. Who developed the basic architecture of computer?

(A) Blaise Pascal

(B) Charles Babbage

(C) John Von Neumann

(D) None of these

14. The ALU of a computer responds to the commands coming from

(A) Primary memory

(B) Control sections

(C) External memory

(D) All of the above

15. In CISC architecture most of the complex instructions are stored in ---------

(A) Register

(B) Transistors

(C) Diodes

(D) CMOS

16. What does the hardwired control generator consists of?

(A) Decoder/encoder

(B) Condition codes

(C) Control step counter

(D) All of the mentioned

17. Which type of memory stores data currently being processed by the CPU?

(A) Hard Drive

(B) ROM

(C) RAM

(D) Cache Memory

18. TRAP is a _____ interrupt which has the _____ priority among all other interrupts.

(A) Maskable, lowest

(B) Maskable, highest

(C) Non-maskable, highest

(D) All of the above

19. IEEE stands for _____

(A) Instantaneous Electrical Engineering

(B) Institute of Emerging Electrical Engineers

(C) Institute of Emerging Electronic Engineer's

(D) Institute of Electrical and Electronics Engineers.

20. DMA (Direct Memory Access) transfer data between

(A) Memory and processor

(B) Processor and I/O devices

(C) I/O devices and memory

(D) All of these

21. Which of the following is the hardware mechanism that allow a device to notify the CPU?

(A) Polling

(B) Interrupt

(C) Driver

(D) All of these

22. A storage area used to store data to a compensate for the difference in speed at which the different units can handle data is

(A) Memory

(B) Buffer

(C) Accumulator

(D) Address

23. Which of the following statement is false about dynamic RAM?

(A) DRAM needs a continuously refreshed memory to store data

(B) It is slower than SRAM

(C) It is more expensive than SRAM

(D) All are correct

24. Which of the following is not part of microinstruction code format?

(A) SB

(B) BR

(C) CD

(D) AD

25. If more than one channel requests service simultaneously, the transfer will occur as

(A) Multitransfer

(B) Simultaneous transfer

(C) Burst transfer

(D) None of the above

26. The memory blocks are mapped on to the cache with the help of --------

(A) Hash function

(B) Vectors

(C) Mapping function

(D) None of these

27. To indicate the I/O device that its request for the DMA transfer has been honored by the CPU, the DMA controller pulls

(A) HLDA signal

(B) HRQ signal

(C) DACK (active low)

(D) ACK (active high)

28. Operating system is used in which generation of computer for the first time?

(A) First Generation

(B) Second Generation

(C) Third Generation

(D) Fourth Generation

29. A computer consists of

(A) A central processing unit

(B) A memory

(C) I/O unit

(D) All of the above

30. A set of flip flops integrated together is called-

(A) Counter

(B) Adder

(C) Register

(D) None of the above

31. Which is used for manufacturing chips?

(A) BUS

(B) Countrol Unit

(C) Memory

(D) Semiconductors

32. A register organized to allow to move left or right operations is called a ---

---

(A) Counter

(B) Loader

(C) Adder

(D) Shift register

33. What is the binary representation of the decimal number 13?

(A) 1011

(B) 1101

(C) 1111

(D) 1001

34. 2's complement of the binary number 11001 is:

(A) 00111

(B) 00110

(C) 11001

(D) 00101

35. Which of the following is correct about 8086 microprocessor?

(A) Intel's first X86 processor

(B) Motrola's first X86 processor

(C) STMICROELECTRONICS's first X86 processor

(D) NanoxploreX86 processor

36. In 8086 microprocessor, the address but is ---------- bit wide

(A) 12 bit

(B) 10 bit

(C) 16 bit

(D) 20 bit

37. The CF is known as ----------

(A) Carry flag

(B) Condition flag

(C) Common flag

(D) Single flag

38. The index register are used to hold ----------

(A) Segment memory

(B) Offset memory

(C) Memory register

(D) Offset address

39. Which of the following is not an arithmetic instruction?

(A) INC (increment)

(B) CMP (compare)

(C) DEC (decrement)

(D) ROL (rotate left)

40. Which of the following is the fastest means of memory access for CPU?

(A) Registers

(B) Cache

(C) Main memory

(D) Virtual memory

41. The boot sector files of the system are stored in which computer memory?

(A) Cache

(B) Register

(C) RAM

(D) ROM

42. RAM is ------ and -------

(A) Volatile, temporary

(B) Non-volatile, temporary

(C) Volatile, permanent

(D) Non-volatile, permanent

43. How many bits are in a byte?

(A) 4

(B) 8

(C) 16

(D) 32

44. Which of the following is the largest value that can be represented using 8 bits?

(A) 255

(B) 128

(C) 512

(D) 64

45. What is the output of an AND gate if both inputs are set to logic HIGH (1)?

(A) 0

(B) 1

(C) X

(D) Depends on gate parameters

46. What is the output of an XOR gate it both inputs are set to logic HIGH (1)?

(A) 0

(B) 1

(C) X

(D) Depends on gate parameters

47. What is the primary function of the control unit in a computer?

(A) Execute arithmetic operations

(B) Store data temporarily

(C) Control the flow of data within the CPU

(D) Perform logical comparisons

48. What is the purpose of the CPU cache?

(A) Store frequently accessed data and instructions to speed up processing

(B) Provide long-term storage for programs and files

(C) Execute arithmetic operations

(D) Control the input/output operations of the computer

49. Which of the following components is responsible for temporarily storing data and instructions during program execution?

(A) Cache Memory

(B) RAM (Random Access Memory)

(C) Hard Disk Drive (HDD)

(D) ROM (Read Only Memory)

50. Which component of the CPU is responsible for fetching instructions from memory?

(A) Arithmetic Logic Unit (ALU)

(B) Control Unit

(C) Cache Memory

(D) Registers

51. Which programming language is primarily used to program the basic computer?

(A) C

(B) Java

(C) Assembly language

(D) Python

52. What is the purpose of a loader in programming the basic computer?

(A) Translate high-level language code into machine language

(B) Load the program into memory for execution

(C) Convert the program into assembly language

(D) Manage input/output operations

53. Which of the following is NOT a type of volatile memory?

(A) RAM (Random Access Memory)

(B) ROM (Read Only Memory)

(C) Cache Memory

(D) Registers

54. Which of the following is an example of an input device?

(A) Printer

(B) Monitor

(C) Keyboard

(D) Speaker

55. What is the primary function of input/output devices in a computer system?

(A) Execute program instructions

(B) Perform arithmetic and logical operations

(C) Store data and program instructions

(D) Enable communication between the computer and the external world

56. A computer using more than one CPU at a time is called ----------

(A) Multiprogramming

(B) Multiprocessing

(C) Multitasking

(D) Multitherading

57. What is the primary function of an assembler in programming the basic computer?

(A) Translate high-level language code into machine language

(B) Translate assembly language code into machine language

(C) Execute the program instructions

(D) Debug the program code

58. User communicates with a computer wit the help of which devices.

(A) Input Devices

(B) Output Devices

(C) Software Devices

(D) Both (A) and (B)

59. The CISC stand for

(A) Computer Instruction Set Compliment

(B) Complete Instruction Set Compliment

(C) Computer Indexed Set Components

(D) Complex Instruction Set Computer

60. A machine language instruction format consists of

(A) Operand field

(B) Operation code field

(C) Operation code field & operand field

(D) None of these

61. How many address lines and input-output data line are needed for the 64×8 memory unit

(A) 16 address line, 3 data line

(B) 6 address line, 3 data line

(C) 60 address line, 8 data line

(D) 16 address line, 8 data line

62. The number successful accesses to memory state as a fraction is called as --------

(A) Hit Rate

(B) Miss Rate

(C) Success Rate

(D) Access Rate

63. The key characteristics of Microprogrammed control is?

(A) Expensive

(B) Complex Hardware

(C) RISC

(D) Flexibility of adding new instruction

64. Which algorithm associates with each page the time when the page was brought into memory

(A) Optimal Page replacement

(B) First-In-First-Out

(C) LRU replacement algorithm

(D) Counting based replacement

65. On subtracting +28 from +29 using 2's complement we get ---------

(A) 11111010

(B) 11110101

(C) 100001

(D) 1

66. In floating point representation the part represents a signed & fixed point number is called as?

(A) Exponent

(B) Mantissa

(C) Normalized

(D) Float

67. The Generation based on VISI microprocessor.

(A) 1st generation

(B) 2nd generation

(C) 3rd generation

(D) 4th generation

68. Both the CISC and RISE architectures have been developed to reduce the --------

(A) Time delay

(B) Semantic gap

(C) Cost

(D) All of these

69. Which addressing mode is most suitable to change the normal sequence of executing of instruction

(A) Relative addressing mode

(B) Indirect addressing mode

(C) Direct addressing mode

(D) Immediate addressing mode

70. Serial transmission without stop bits, start bits or gaps is called ---------- transmission.

(A) Parallel

(B) Synchronous

(C) Asynchronous

(D) Virtual

71. The ALU gives the output of the operation and the output is stored in the -------

(A) Memory Devices

(B) Register

(C) Flags

(D) Output unit

72. Which computer work on data in 0's and 1's

(A) Digital computer

(B) Hybrid computer

(C) Physical computer

(D) Analog computer

73. Which of the following memories has the fastest (or shortest) access time?

(A) RAM

(B) ROM

(C) Magnetic Core Memory

(D) Cache memory

74. Computer data is transmitted block by block in transmission known as

(A) Syncronous

(B) Digital

(C) Asyncronous

(D) Analog

75. Which of the architecture is power efficient?

(A) ISA

(B) IANA

(C) RISC

(D) CISC